FIG. 1

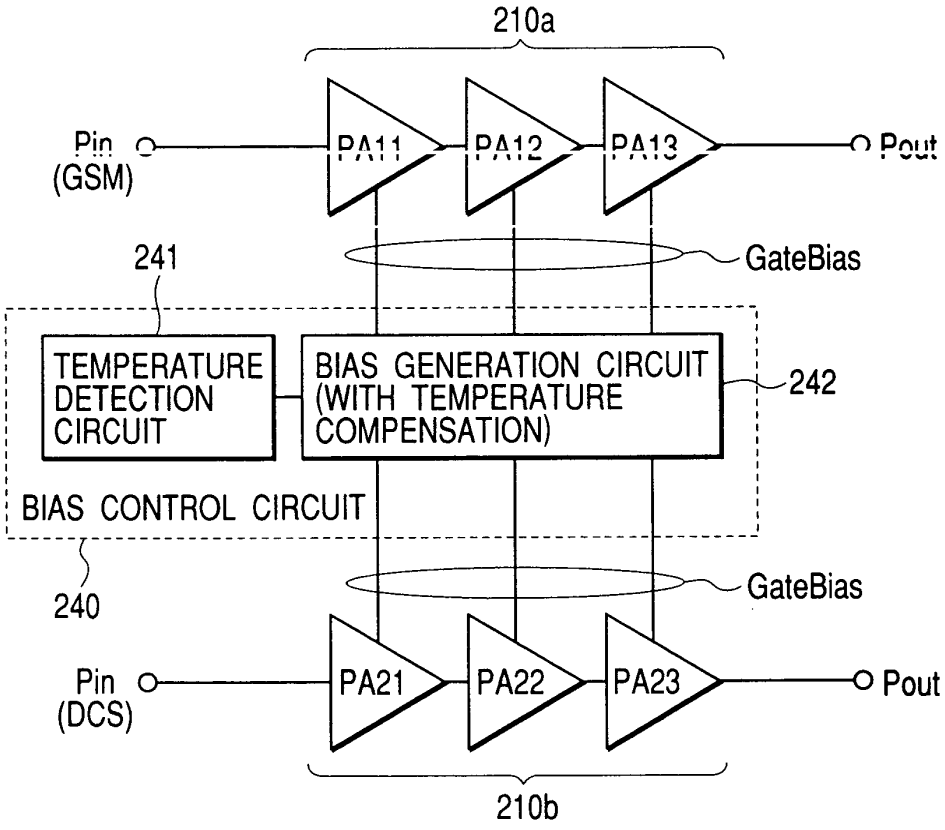

210a
Pin
(GSM)
PA11
PA12
PA13
Pout
241
GateBias
TEMPERATURE
DETECTION
CIRCUIT
BIAS GENERATION CIRCUIT
(WITH TEMPERATURE
COMPENSATION)
242
BIAS CONTROL CIRCUIT
240
GateBias
Pin
(DCS)
PA21
PA22
PA23
Pout
210b

FIG. 2

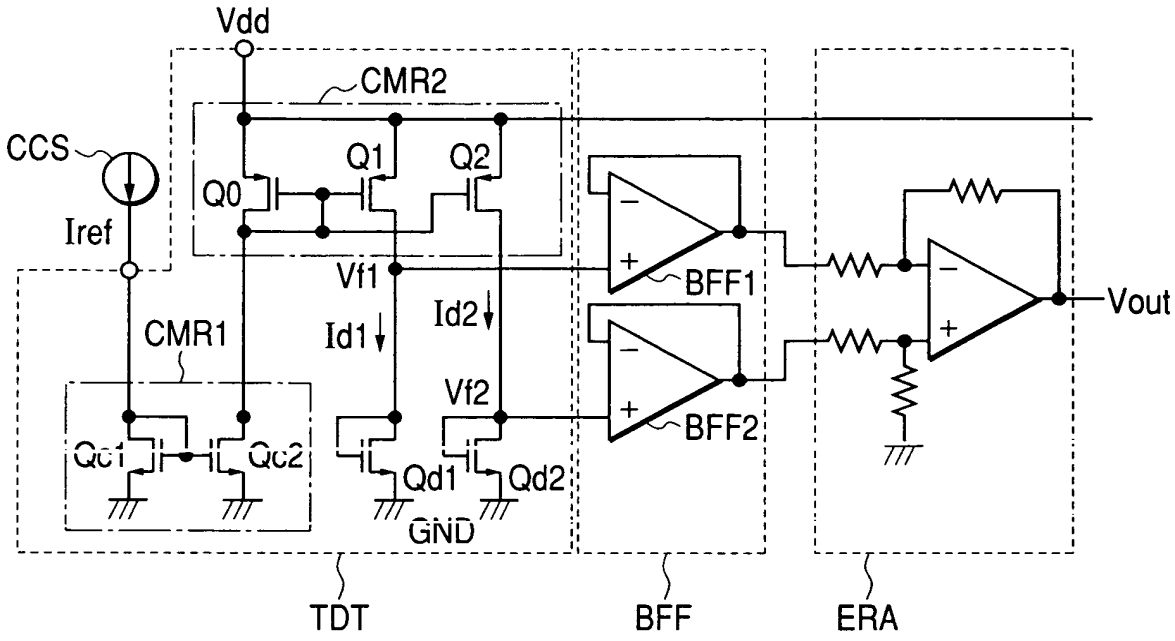

Vdd
CMR2
CCS
Q1
Q2
Q0
Iref
Vf1
Id1
Id2
BFF1
Vout
CMR1
Vf2
BFF2
Qc1
Qc2
Qd1
Qd2
GND
TDT
BFF
ERA

FIG. 3

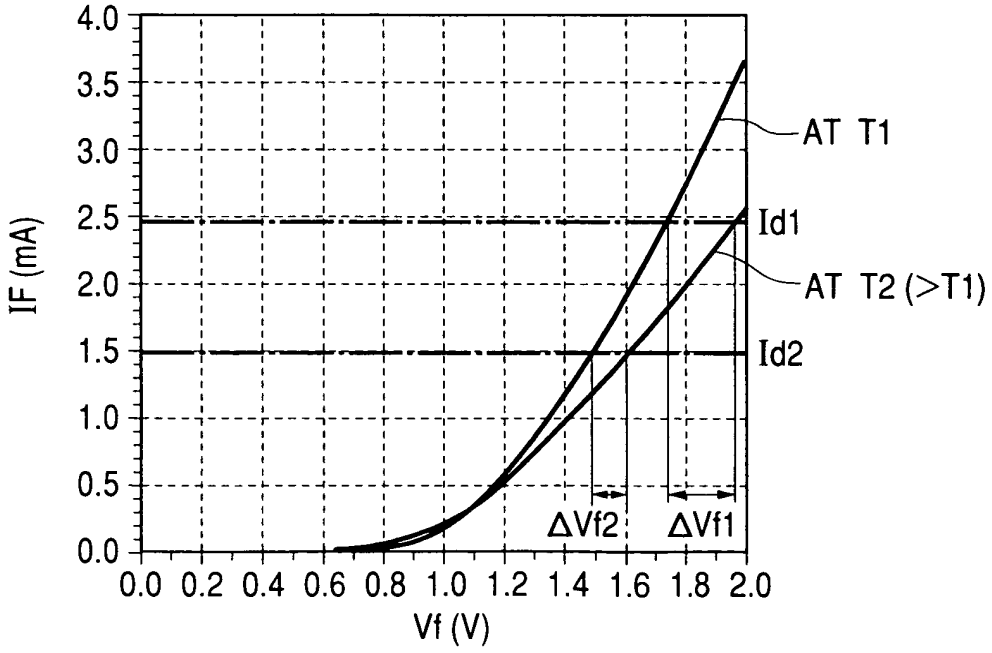

4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
IF (mA)
AT T1
Id1
AT T2 (>T1)
Id2
ΔVf2
ΔVf1
0.0 0.2 0.4 0.6 0.8 1.0 1.2 1.4 1.6 1.8 2.0
Vf (V)

FIG. 4

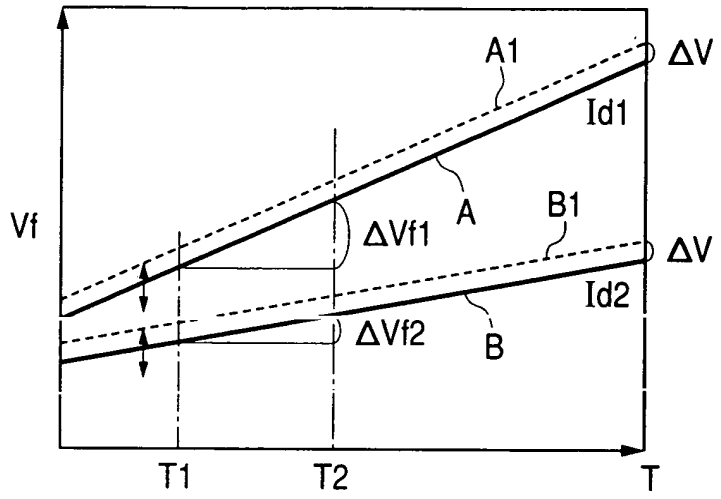


FIG. 5

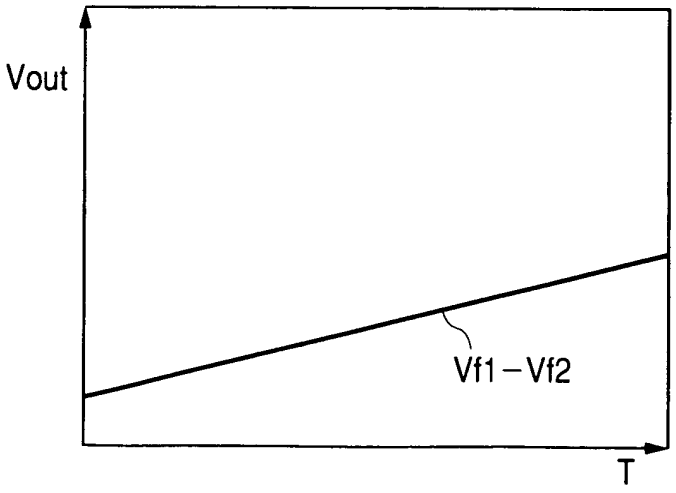


FIG. 6

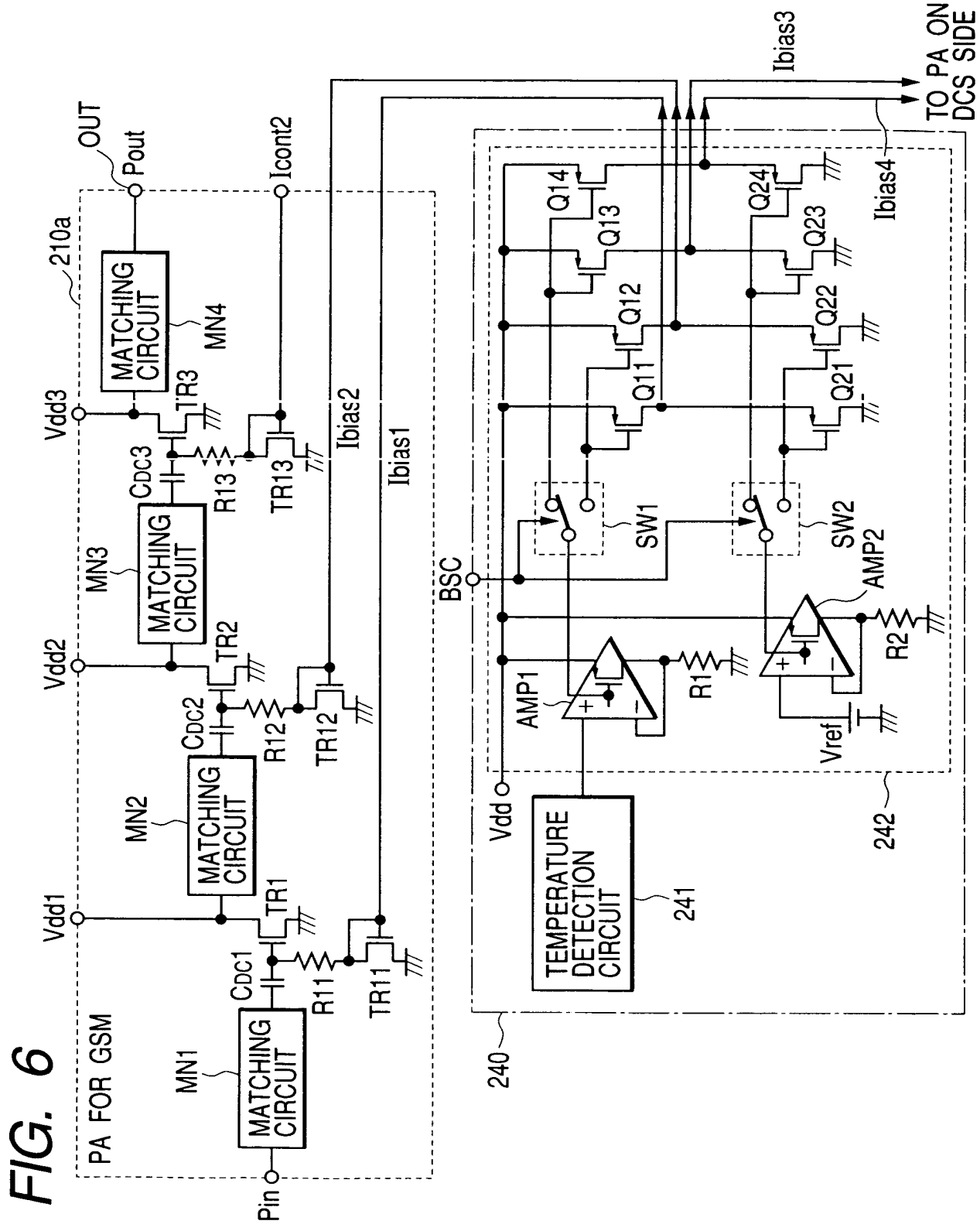

PA FOR GSM
210a
OUT
Pout
Pin
Vdd1
Vdd2
Vdd3
MN1
MN2
MN3
MN4
MATCHING CIRCUIT
TR1
TR2
TR3
TR11
TR12
TR13
R11
R12
R13
CDC1
CDC2
CDC3
Icont2
Ibias1
Ibias2
Ibias3
Ibias4
TO PA ON DCS SIDE
BSC
Vdd
240
241
242
TEMPERATURE DETECTION CIRCUIT
AMP1
AMP2
SW1
SW2
R1
R2
Vref
Q11
Q12
Q13
Q14
Q21
Q22
Q23
Q24

FIG. 7

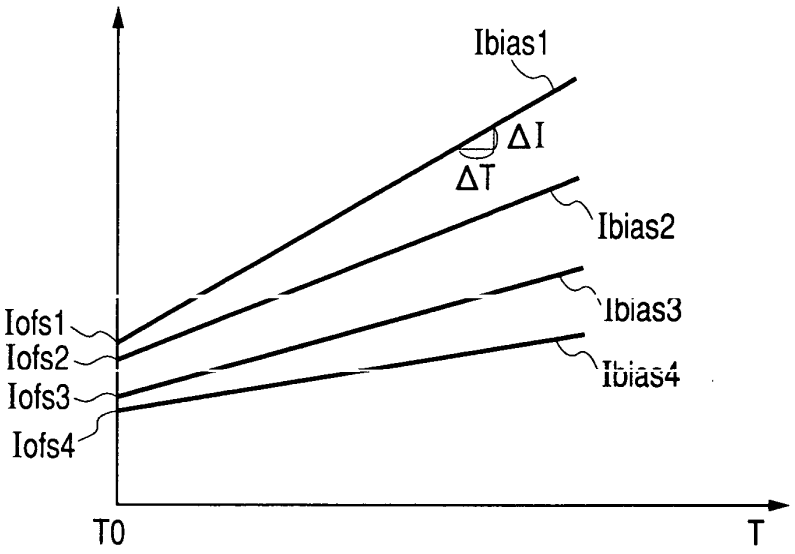

Ibias1
ΔI
ΔT
Ibias2
Ibias3
Ibias4
Iofs1
Iofs2
Iofs3
Iofs4
T0
T

FIG. 8

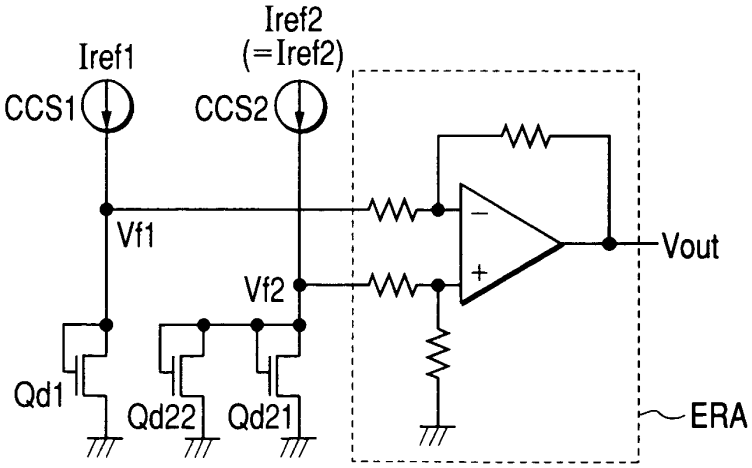

Iref2
(=Iref2)
Iref1
CCS1
CCS2
Vf1
Vf2
Vout
Qd1
Qd22
Qd21
ERA

FIG. 9

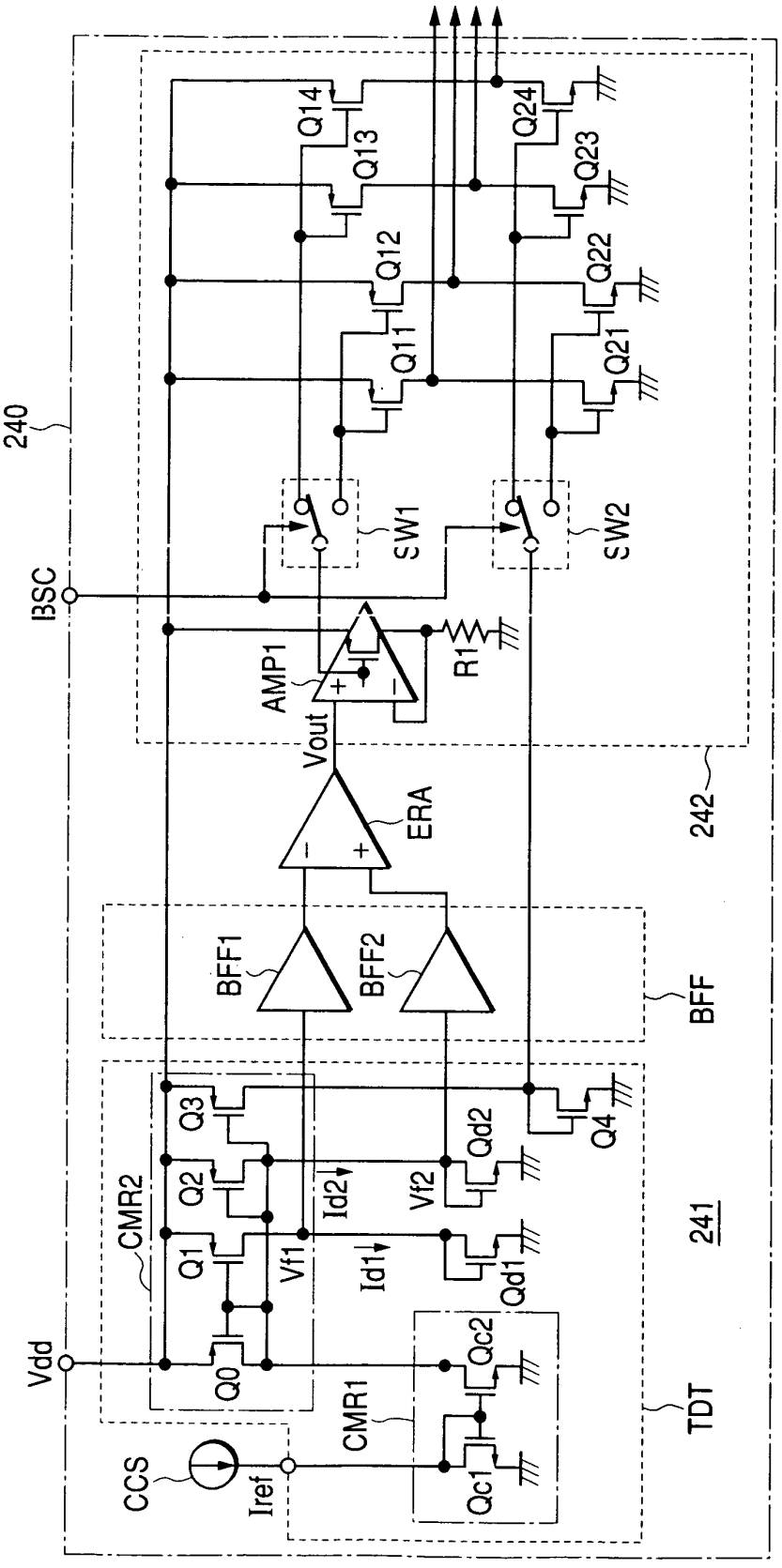

240
BSC
SW1
SW2
Q14
Q13
Q12
Q11
Q24
Q23
Q22
Q21
AMP1
R1
Vout
ERA
242
BFF1
BFF2
BFF
Q3
Q2
Q1
Q0
CMR2
Vf1
Id2
Id1
Vf2
Qd2
Qd1
Q4
241
Vdd
CCS
Iref
CMR1
Qc2
Qc1
TDT

FIG. 10

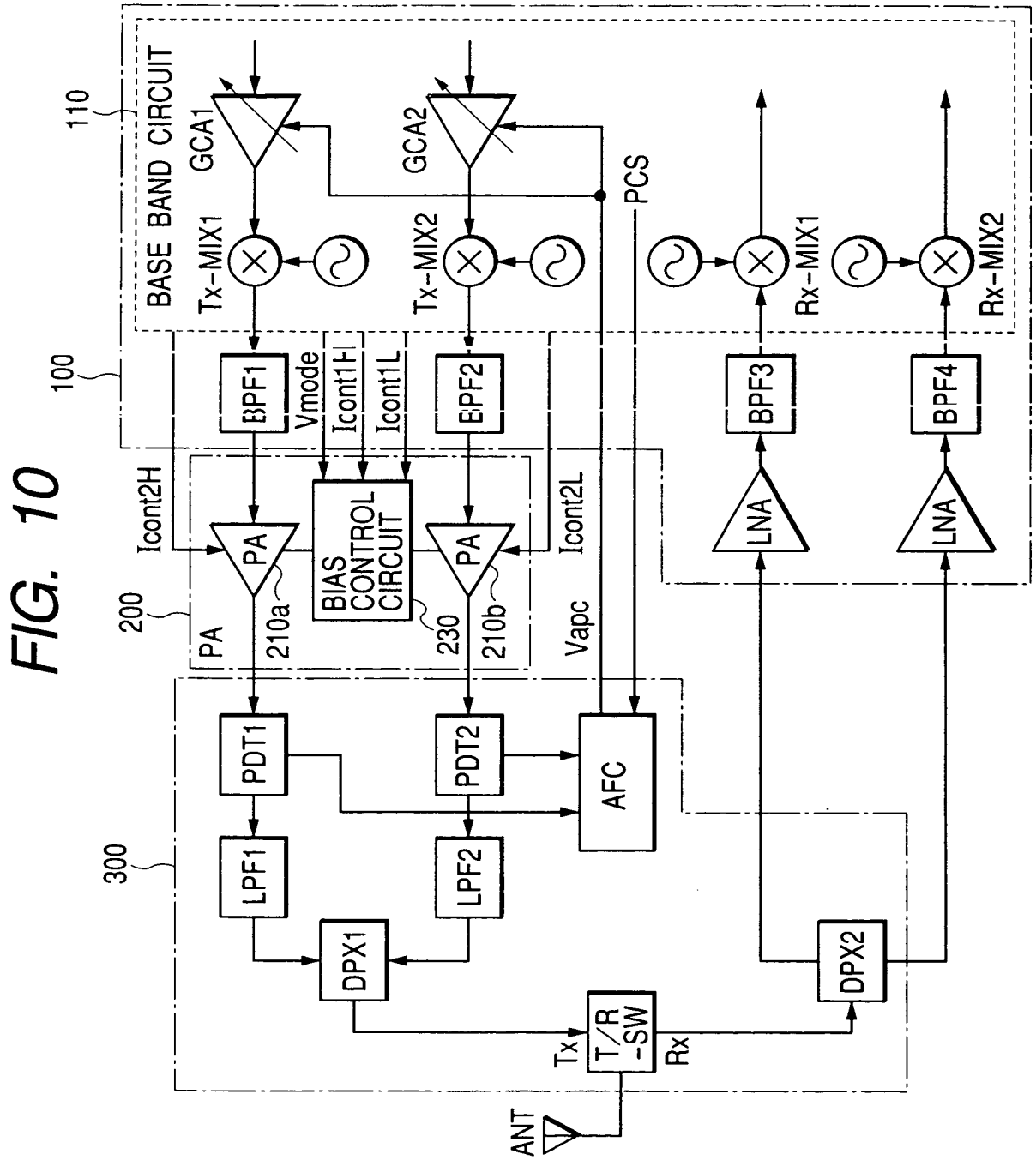

110
BASE BAND CIRCUIT
GCA1
GCA2
PCS
Tx-MIX1
Tx-MIX2
Rx-MIX1
Rx-MIX2
100
BPF1
Vmode
Icont1H
Icont1L
BPF2
BPF3
BPF4
Icont2H
Icont2L
PA
BIAS CONTROL CIRCUIT
LNA
200
PA
210a
230
210b
Vapc
300
PDT1
PDT2
AFC
LPF1
LPF2
DPX1
DPX2
Tx
T/R -SW
Rx
ANT

FIG. 11

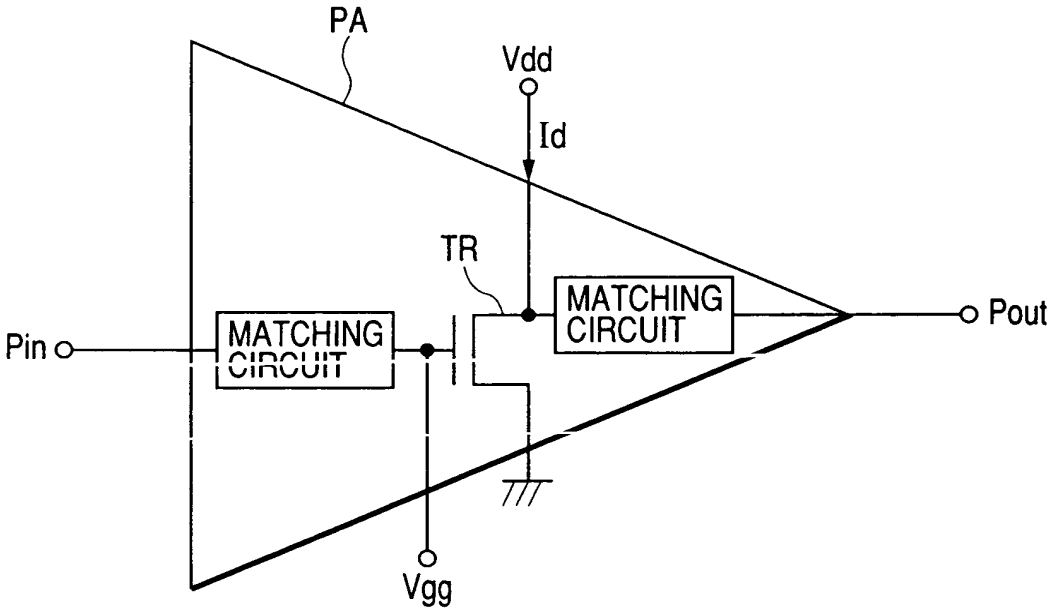
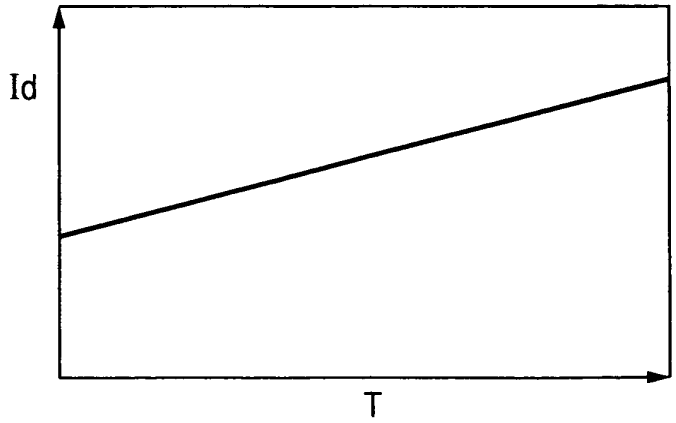

PA
Vdd
Id
TR
MATCHING CIRCUIT
Pout
Pin
MATCHING CIRCUIT
Vgg

FIG. 12


Id
T